CLAIM AMENDMENTS:

Please add new claims 37-40 so that a complete list of the currently pending claims reads as follows.

1-20. (Cancelled)

21. (Original) A method, comprising:

operating a microprocessor to generate a first set of at least two address bit signals, said first set of at least two address bit signals being indicative of a first cache configuration; and

operating said microprocessor to generate a second set of at least two address bit signals, said second set of at least two address bit signals being indicative of said second cache configuration of said plurality of cache configurations.

22. (Original) The method of claim 21, further comprising:

operating a microprocessor to select said first cache configuration of a plurality of cache configurations;

operating said microprocessor to provide a control signal indicative of said selection of said first cache configuration; and

operating said microprocessor to concurrently provide said first set of at least two address bit signals to a first memory device and a second memory device in response to said control signal.

23. (Original) A method, comprising:

operating a microprocessor to select a first cache configuration of a plurality of cache configurations; and

subsequently operating said microprocessor to concurrently provide a set of at least two address bit signals to a first memory device and a second memory device, said set of at least two address bit signals being representative of said selection of said first cache configuration.

24. (Original) The method of claim 23, further comprising:

operating a microprocessor to provide a control signal indicative of a said selection of a first cache configuration, said operating of said microprocessor to concurrently provide said set of at least two address bit signals to said first memory device and said second memory device is in response to said control signal.

25 – 27. (Cancelled)

28. (Previously Presented) A method of operating a microprocessor for supporting multiple cache configurations, the method comprising:

generating a first set of at least two address bit signals indicative of a first cache configuration among the multiple cache configurations; and

generating a second set of at least two address bit signals indicative of a second cache configuration among the multiple cache configurations.

29. (Previously Presented) The method of claim 28, further comprising:

selecting the first cache configuration during a first boot of the microprocessor; and

communicating the first set of at least two address bit signals to a first memory device and a second memory device as an indication of the selection of the first cache configuration among the multiple cache configurations during the first boot of the microprocessor.

30. (Previously Presented) The method of claim 29, further comprising:

selecting the second cache configuration during a second boot of the microprocessor; and

communicating the second set of at least two address bit signals to the first memory device and the second memory device as an indication of the selection of the second cache configuration among the multiple cache configurations during the second boot of the microprocessor.

31-32. (Cancelled)

33. (Previously Presented) In a microprocessor including a controller and a multiplexor, a method of operating the microprocessor for supporting multiple cache configurations, the method comprising:

operating the controller to generate a first set of at least two address bit signals indicative of a first cache configuration among the multiple cache configurations;

operating the controller to generate second set of at least two address bit signals indicative of a second cache configuration among the multiple cache configurations; and

operating the multiplexor to selectively communicate either the first set of at least two address bit signals or the second set of at least two address bit signals to a first memory device and a second memory device,

wherein a communication of the first set of at least two address bit signals to the first memory device and the second memory device is an indication of a selection of the first cache configuration during a boot of the microprocessor, and

wherein a communication of the second set of at least two address bit signals to the first memory device and the second memory device is an indication of a selection of the second cache configuration during the boot of the microprocessor.

34. (Previously Presented) In a microprocessor including a controller and a multiplexor, a method of operating the microprocessor for supporting multiple cache configurations, the method comprising:

operating the controller to generate a first set of at least two address bit signals indicative of a first cache configuration among the multiple cache configurations; and

operating the multiplexor to communicate the first set of at least two address bit signals to a first memory device and a second memory device as an indication of a selection of the first cache configuration during a first boot of the microprocessor.

35. (Previously Presented) The method of claim 34, further comprising:

operating the controller to generate a second set of at least two address bit signals indicative of a second cache configuration among the multiple cache configurations; and

operating the multiplexor to communicate the second set of at least two address bit signals to the first memory device and the second memory device as an indication of a selection of the second cache configuration during a second boot of the microprocessor.

36. (New) The method of claim 21 wherein the configuration of the cache represents a size of the cache.

37. (New) A method, comprising:

operating a microprocessor to generate a first set of at least two address bit signals, said first set of at least two address bit signals being indicative of a first cache configuration; and

operating said microprocessor to generate a second set of at least two address bit signals, said second set of at least two address bit signals being indicative of said second cache configuration of said plurality of cache configurations; and

operating said microprocessor to send the first and second set of address bit signals to a first and second memory device, the first memory device including a first and second address pin and the second memory device including a third and fourth address pin, wherein said first address pin and said fourth address pin are electrically coupled to thereby concurrently receive a first address bit signal, and wherein said second address pin and said third address pin are electrically coupled to thereby concurrently receive a second address bit signal.

38. (New) The method of claim 37 wherein the cache configuration represents a size of the cache.

39. (New) The method of claim 37 further comprising:

selecting the first cache configuration during a first boot of the microprocessor; and

communicating the first set of at least two address bit signals to the first memory device and the second memory device as an indication of the selection of the first cache configuration among the multiple cache configurations during the first boot of the microprocessor.

40. (New) The method of claim 39 further comprising:

selecting a second cache configuration among the multiple cache configurations during a second boot of the microprocessor; and

communicating the selection of the second cache configuration among the multiple cache configurations during the second boot of the microprocessor to the first memory device and the second memory device.